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| EXAMINER | |
|---|---|
| TO, JENNIFER N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2195 | |

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| 11/21/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/763,777 | GOSALIA ET AL. | |
| | Examiner | Art Unit | |
| | JENNIFER N. TO | 2195 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *15-51,66,68-73 and 80-91* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-40 and 80-91* is/are allowed.

6)☒ Claim(s) *41-43,45,48,50,51,66 and 69-73* is/are rejected.

7)☒ Claim(s) *44,46,47,49 and 68* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/11/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 15-51, 66, 68-73, and 81-91 are pending for examination.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 41-43, 45, 48, 51, 66, 69, 70-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (U.S. Patent No. 5760789), and in view of Hagemark et al. (hereafter Hagemark) (U.S. Patent No. 6070002).

4. Inoue was cited in the previous office action.

5. As per claim 41, Inoue teaches the invention substantially as claimed including an apparatus for supporting scheduling of tasks for processing by a coprocessor, comprising:

a central processing unit (CPU) (col. 10, lines 6-8);

a coprocessor (col. 10, lines 8-9);

one or more applications that generate tasks for processing by the coprocessor wherein the tasks are first stored in a user mode command buffer (col. 8, lines 50-58);

a scheduler process for determining an order in which the tasks are processed; wherein the order accounts for any relative priority among a first application relating to a first set of tasks and one or more other applications relating to additional tasks, and the order accounts for a corresponding amount of processing time that the first application and one or more other applications are entitled to (Column 12, lines 5-17).

6. Inoue did not specifically teach that wherein said tasks are stored in a per-application context in said user mode command buffer.

7. However, Hagemark teaches that wherein said tasks are stored in a per-application context in said user mode command buffer (abstract, lines 3-4, 18-21; col. 3, lines 8-11; col. 5, lines 38-41; col. 6, lines 4-10).

8. It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have combined the teaching of Inoue and Hagemark because Hagemark teaching of storing tasks in user mode command buffer in per-application context would improved the flexibility of Inoue's system (Hagemark, col. 15, lines 9-10) by expanding the ability of user application to direct the manipulation of real-time video, particularly direct the image conversion processing and graphic processing (Hagmark, col. 5 lines 15-21).

9. As per claim 42, the combined Inoue and Hagemnark teach the invention as claimed including wherein the coprocessor is a GPU (Inoue, col. 10, lines 8-9).

10. As per claim 43, the combined Inoue and Hagemark teach the invention as claimed including wherein the coprocessor supports interruption during the processing of a task by automatically saving task information to a coprocessor-accessible memory location (Inoue, Column 8, lines 59-67, column 9, lines 1-14 and Column 12, line 24-29).

11. As per claim 45, the combined Inoue and Hagemark teach the invention as claimed including wherein the coprocessor is capable of storing information regarding the history of coprocessor switches from task to task in a specified system memory location readable by the scheduler process (Inoue, col. 8, lines 59-67, col. 9, lines 1-14; col. 12, lines 24-29).

12. As per claim 48, the combined Inoue and Hagemark did not specifically teach that wherein the coprocessor specifies a write pointer for indicating where in the system memory location the coprocessor should write to next. However, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to have recognized that in order to write to memory, one needs to specify a location in memory to write to by creating a pointer to that memory location.

13. As per claim 51, the combined Inoue and Hagemark teach context switching between input hardware queue tasks and client tasks (Inoue, col. 9, lines 1-14). The combined Inoue and Hagemark did not specifically teach that wherein the coprocessor supports enable/disable context switching instructions such that when context switching is disabled, the coprocessor will not switch away from a current coprocessor task. However, it would have been obvious at the time of the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have enabled and disabled context switching if input hardware tasks were not high priority tasks, and where all the tasks of one particular source, i.e. Client 1, Client 2, Input Hardware, were allowed to be executed until completion.

14. As per claim 66, it is rejected for the same reason as claim 41 above. In addition the combined Inoue and Hagemark teach a coprocessor (Inoue, col. 10, lines 8-9) for use in connection with a coprocessing scheduler (Inoue, col. 12, lines 5-17), comprising: a coprocessor for processing tasks that are initially gathered in a user mode command buffer memory group(Inoue, col. 8, lines 50-58), and wherein said tasks are submitted to the coprocessor by a scheduler process that submits tasks to the coprocessor according to a priority of applications relating to said tasks and that request processing of the tasks, and wherein the priority determines the amount of coprocessor time one or more applications are entitled to (Inoue, col.12, lines 5-17).

15. As per claim 69, the combined Inoue and Hagemark teach that wherein the coprocessor processes tasks from a run list by switching immediately to a subsequent task on the run list when a switching event occurs (Inoue, col. 9, lines 1-14).

16. As per claim 70, the combined Inoue and Hagemark teach that wherein a switching event comprises at least one of a completion of processing a previously submitted task, a page fault in processing a task, a general protection fault in processing a task, and a request by a central processing unit (CPU) to switch to a new run list (Inoue, col. 12, lines 24-29).

17. As per claim 71, the combined Inoue and Hagemnark teach the invention as claimed including wherein the coprocessor is a GPU (Inoue, col. 10, lines 8-9).

18. As per claim 72, the combined Inoue and Hagemark that wherein the coprocessor accesses memory resources in a coprocessor-readable memory by a memory manager (Inoue, col. 9, lines 45-65).

19. As per claim 73, the combined Inoue and Hagemark did not specifically teach that wherein the memory resources comprise references to virtual memory addresses. However, it was well known in the art that buffer memory is virtual memory and therefore it would have been obvious that the memory resources are referenced to virtual memory addresses when accessed.

20. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US 5,760,789) in view of Hagemark et al. (hereafter Hagemark) (U.S. Patent No. 6070002), As applied in claim 41 above, and further in view of Magar et al (US 4,713,748).

21. Inoue and Magar were cited in the previous office action.

22. As per claim 50, the combined of Inoue and Hagemark teaches the invention substantially as claimed in claim 41 above. The combined Inoue and Hagemark did not specifically teach that wherein the coprocessor supports trap instructions that are capable of generating a CPU interrupt when processed by the coprocessor.

23. However Magar teaches wherein the coprocessor supports trap instructions that are capable of generating a CPU interrupt when processed by the coprocessor (col. 68, lines 27-36, i.e. a microprocessor with a trap instruction that acts as a software interrupt to transfer program control to another program memory location).

24. It would have been obvious to one of an ordinary skill in the art at the time of the invention was made to combined the teaching of Inoue, Hagemark and Magar because Magar teaching of using a trap instruction as a software interrupt would improve the integrity of Inoue and Hagemark's system by handling the input hardware queue tasks of the combined Inoue and Hagemark's system at the graphics processor instead of

having to check for input hardware queue instructions periodically at the queue buffer/server queue. This would further improve hardware input response and simplify the "Dispatch" routine.

***Allowable Subject Matter***

25. Claims 44, 46, 47, 49 and 68 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

26. Claims 15-40 and 80-91 are allowabled.

***Response to Arguments***

27. Applicant's arguments with respect to claims 41-43, 45, 48, 50, and 51 have been considered but are not persuasive in view of the new ground(s) of rejection.

***Conclusion***

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JENNIFER N. TO whose telephone number is (571)272-7212. The examiner can normally be reached on M-T 6AM- 3:30 PM, F 6AM- 2:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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